CLAIMS

What is claimed is:

1. An integrated circuit structure comprising:

a substrate;

a plurality of different height devices positioned on said substrate;

a passivating layer positioned above said substrate and between said devices;

a wiring layer above said passivating layer,

wherein at least one of the tallest of said plurality of devices is in direct contact with said wiring layer and at least one of the shorter of said plurality of devices is connected to said wiring layer by a first contact extending through said passivating layer.

2. The integrated circuit in claim 1 wherein said at least one of the tallest of said plurality of devices is in direct contact with a first second contact in said wiring layer.

3. The integrated circuit in claim 2, further comprising a via layer above said wiring layer, wherein said second contact is directly connected to said via layer.

4. The integrated circuit in claim 3, wherein said second contact extends through said wiring layer to said via layer.

5. The integrated circuit in claim 3, wherein said second contact is positioned within said wiring layer.

6. The integrated circuit in claim 1 wherein said wiring layer further comprises wiring within said wiring layer.

7. The integrated circuit in claim 6 wherein said first contact is connected to said wiring in said wiring layer.

8. The integrated circuit in claim 6, wherein said at least one of the tallest of said plurality of devices is in direct contact with a first second contact in said wiring layer and said second contact within said wiring layer comprises a different material than said wiring within said wiring layer.

9. The integrated circuit in claim 1, wherein said at least one of the tallest of said plurality of devices comprises a different type of device than said at least one of the shorter of said plurality of devices.

10. The integrated circuit in claim 1, wherein the top of said at least one of the tallest of said plurality of devices is substantially coplanar with the top of said passivating layer.

11. The integrated circuit in claim 10, wherein the top of said passivating layer is at a height within about 50 nanometers from the top of said at least one of the tallest of said plurality of devices.

12. A method of forming the integrated structure in claim 1 comprising the steps of:

providing a substrate;

forming a plurality of different height devices positioned on said substrate;

forming a passivating layer positioned above said substrate and between said devices;

removing a portion of said passivating layer to expose the top of at least one of the tallest of said plurality of devices while leaving the shorter of said plurality of devices covered by said passivating layer;

forming said first contact in said passivating layer, said first contact connected to said at least one of the shorter of said plurality of devices; and

forming a wiring layer above said passivating layer such that said wiring layer is in direct contact with said top of said at least one of the tallest of said plurality of devices.